GX3700

FPGA PXI HIGH-PERFORMANCE DIGITAL I/O CARD

- User configurable, on-board Altera Stratix III FPGA
- No proprietary FPGA design tools required
- Compatible with Altera's free, web-based Quartus II design tools
- 160 digital I/O signals available for user specific applications
- 700 MHz digital I/O clock rate
- · Supports user defined expansion boards for custom interfaces



DESCRIPTION

The GX3700 is a user configurable, FPGA-based, 3U PXI card which offers 160 digital I/O signals which can be configured for single-ended or differential interfaces. The card employs the Altera Stratix III FPGA, which can support SerDes data rates up to 1.2 Gb/s, digital I/O clock rates of 700 MHz, and features over 45,000 logic elements and 1.836 Kb of memory. The GX3700 is supplied with an integral expansion board providing access to the FPGA's 160 I/Os. Alternatively, users can design their own custom expansion cards for specific applications - eliminating the need for additional external boards which are cumbersome and physically difficult to integrate into a test system. The design of the FPGA is done by using Altera's free Quartus II Web Edition tool set. Once the user has compiled the FPGA design, the configuration file can be loaded into the FPGA directly or via an on-board EEPROM.

FEATURES

The GX3700's digital I/O signals are 5 V tolerant. Logic families supported by the I/O interface include LVTTL, LVDS and LVCMOS. The FPGA device supports up to four phase lock loops for clock synthesis, clock generation and for support of the I/O interface. An on-board 80 MHz oscillator is available for use with the FGPA device or alternatively, the PXI 10 MHz clock can be used as a clock reference by the FPGA.

The FPGA has access to all of the PXI bus resources including the PXI 10 MHz clock, the local bus, and the PXI triggers; allowing the user to create a custom instrument which incorporates all PXI bus resources. Control and access to the FPGA is provided via the GX3700's driver which includes DMA and interrupt support tools for downloading the compiled FPGA code as well as register read and write functionality.

PROGRAMMING AND SOFTWARE

The board is supplied with the GXFPGA library, a software package that includes a virtual instrument panel, and a Windows 32/64-bit DLL driver library and documentation. The virtual panel can be used to interactively program and control the instrument from a window that displays the instrument's current settings and status. In addition, interface files are provided to support access to programming tools and languages such as ATEasy, LabView, LabView/Real-Time, C/C++, Microsoft Visual Basic®, Delphi, and Pascal. An On-Line help file and PDF User's Guide provides documentation that includes instructions for installing, using and programming the board.

A separate software package - $\underline{GtLinux}$ - provides support for Linux 32/64 operating systems.

APPLICATIONS

- Automatic Test Equipment (ATE)
- Semiconductor test
- Custom interface emulation
- Custom instrumentation
- SerDes interfaces



GX3700

SPECIFICATIONS

DIGITAL I/O CHANNELS		
Logic Families	LVTTL, LVDS, configurable for 1.2 / 2.5 / 3.3 V	
Logio i uninoc	logic;	
	5 V compatible	
Output Current	±4.0 mA	
Input Leakage Current	±10 µA	
Power on State	Default is disconnect at power on (unprogrammed FPGA) or defined by FPGA program	
Number of Channels	160 I/O signals Direction is configurable on a per channel basis Up to 64 I/O can be differential (32 differential channels) (4) I/O are single-ended or (2) differential clock inputs	
Protection	Overvoltage: -0.5 V to 7.0 V (input) Short circuit: up to 8 outputs may be shorted at a time	
Connector	(4) SCSI III, VHDCI type, 68 pin female	
EXPANSION BOARD INTERFACE		
Board ID	4 bits	
External Digital I/O Interface	160, up to 84 differential I/O Can be configured as 42 differential I/O	
Master Clear	From PXI interface	
Power	±12 V, +5 V, +3.3 V, +2.5 V, +1.2 V	
I/O Connector	±12 V, +5 V, +3.3 V, +2.5 V, +1.2 V	
TIMING SOURCES		
PXI Bus		
	10 MHz	
Internal		
Internal FPGA AND MEMO	10 MHz 80 MHz oscillator, ±20 ppm	
	10 MHz 80 MHz oscillator, ±20 ppm	
FPGA AND MEMO	10 MHz 80 MHz oscillator, ±20 ppm RY	
FPGA AND MEMO FPGA Type	10 MHz 80 MHz oscillator, ±20 ppm RY Altera Stratix III, EP3SL50F780	
FPGA AND MEMO FPGA Type Number of PLLs	10 MHz 80 MHz oscillator, ±20 ppm RY Altera Stratix III, EP3SL50F780 Four	
FPGA AND MEMO FPGA Type Number of PLLs Logic Elements	10 MHz 80 MHz oscillator, ±20 ppm RY Altera Stratix III, EP3SL50F780 Four 47.5 K	

(Actual power is de design)	ependent on the specific FPGA and expansion board
3.3 VDC	3.6 A (typ); 4.9 A (max)
5 VDC	0.045 A (max)
12 VDC (For Expansion Board)	Expansion board dependent
ENVIRONMENTAL	-
Operating Temperature	0 °C to +50 °C
Storage Temperature	-20 °C to +70 °C
Relative Humidity (operating)	5% to 80% RH, non-condensing Dew point -5°C - 20°C
Relative Humidity (non-operating)	5% to 95% RH, non-condensing 30°C max
Altitude (operating)	Up to 2000 M
CE Compliance	EN61010-1 EN61326
Size	3U PXI
Weight	200 g

Note: Specifications are subject to change without notice

ORDERING INFORMATION

GX3700	FPGA PXI High-Performance Digital I/O Card
GX3700-M	High-Performance, FPGA PXI Card, (Ruggedized and Conformally Coated)
ACCESSORY	
GT95021	2' Shielded Cable for all 5xxx/35xx (68 Pin)
GT95022	3' Shielded Cable for all 5xxx/35xx (68 Pin)
GT95028	10' Shielded Cable for all 5xxx/35xx (68 Pin)
GT95031	6' Shielded Cable for all 5xxx/35xx (68 Pin)
GX3701	Flex I/O Feed Through Expansion Board for GX3700 / GX3700e FPGA Module

